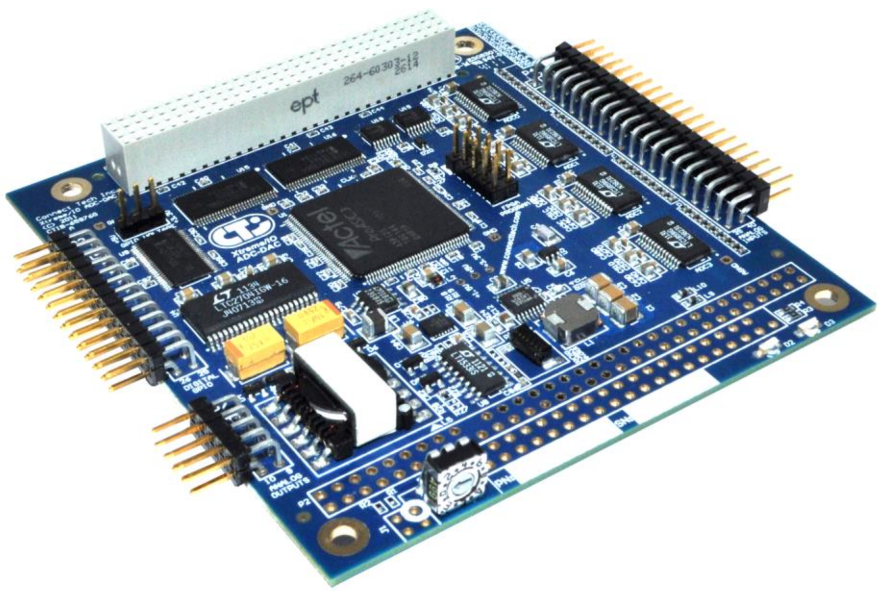
Connect Tech Inc.
Industrial Strength Communications

Xtreme I/O ADC-DAC
User Manual



Connect Tech Inc.
42 Arrow Road
Guelph, Ontario
N1K 1S6

Tel:	519-836-1291
Toll:	800-426-8979 (North America only)
Fax:	519-836-4878
Email:	sales@connecttech.com
	support@connecttech.com
Web:	www.connecttech.com

CTIM-00092 Revision 0.02 – 12/09/2014

Limited Lifetime Warranty

Connect Tech Inc. provides a lifetime warranty for all of our products. Should this product, in Connect Tech Inc.'s opinion, fail to be in good working order during the warranty period, Connect Tech Inc. will, at its option, repair or replace this product at no charge, provided that the product has not been subjected to abuse, misuse, accident, disaster or non Connect Tech Inc. authorized modification or repair.

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Revision History

Revision	Date	Author(s)	Change(s)
0.00	01-03-2012	PD	Initial Manual Revision Created
0.01	03-14-2013	PD	- Fixed DAC Pseudo Code Examples - Fixed GPIO Register Diagram - Added Power Details for Input Power and Current Consumption
0.02	12-09-2014	PD	- Corrected PCI IDs (all should be 0x1201)

Customer Support Overview

If you experience difficulties after reading the manual and/or using the product, contact the Connect Tech Inc. reseller from which you purchased the product. In most cases the reseller can help you with product installation and difficulties.

In the event that the reseller is unable to resolve your problem, our highly qualified support staff can assist you. Our support section is available 24 hours a day, 7 days a week on our website at: www.connecttech.com/sub/support/support.asp. See the contact information section below for more information on how to contact us directly. Our technical support is always free.

Contact Information

We offer three ways for you to contact us:

Mail/Courier

You may contact us by letter at: Connect Tech Inc.
Technical Support
42 Arrow Road, Guelph, ON
Canada N1K 1S6

Email/Internet

You may contact us through the Internet. Our email and URL addresses on the Internet are:
sales@connecttech.com
support@connecttech.com
www.connecttech.com

Note:
Please go to the **Download Zone** or the **Knowledge Database** in the **Support Center** on the Connect Tech Inc. website for product manuals, installation guides, device driver software and technical tips. Submit your technical support questions to our customer support engineers via the **Support Center** on the Connect Tech Inc. website.

Telephone/Facsimile

Technical Support representatives are ready to answer your call Monday through Friday, from 8:30 a.m. to 5:00 p.m. Eastern Standard Time. Our numbers for calls are:

Telephone:	800-426-8979 (North America only)
Telephone:	519-836-1291 (Live assistance available 8:30 a.m. to 5:00 p.m. EST, Monday to Friday)
Facsimile:	519-836-4878 (online 24 hours)

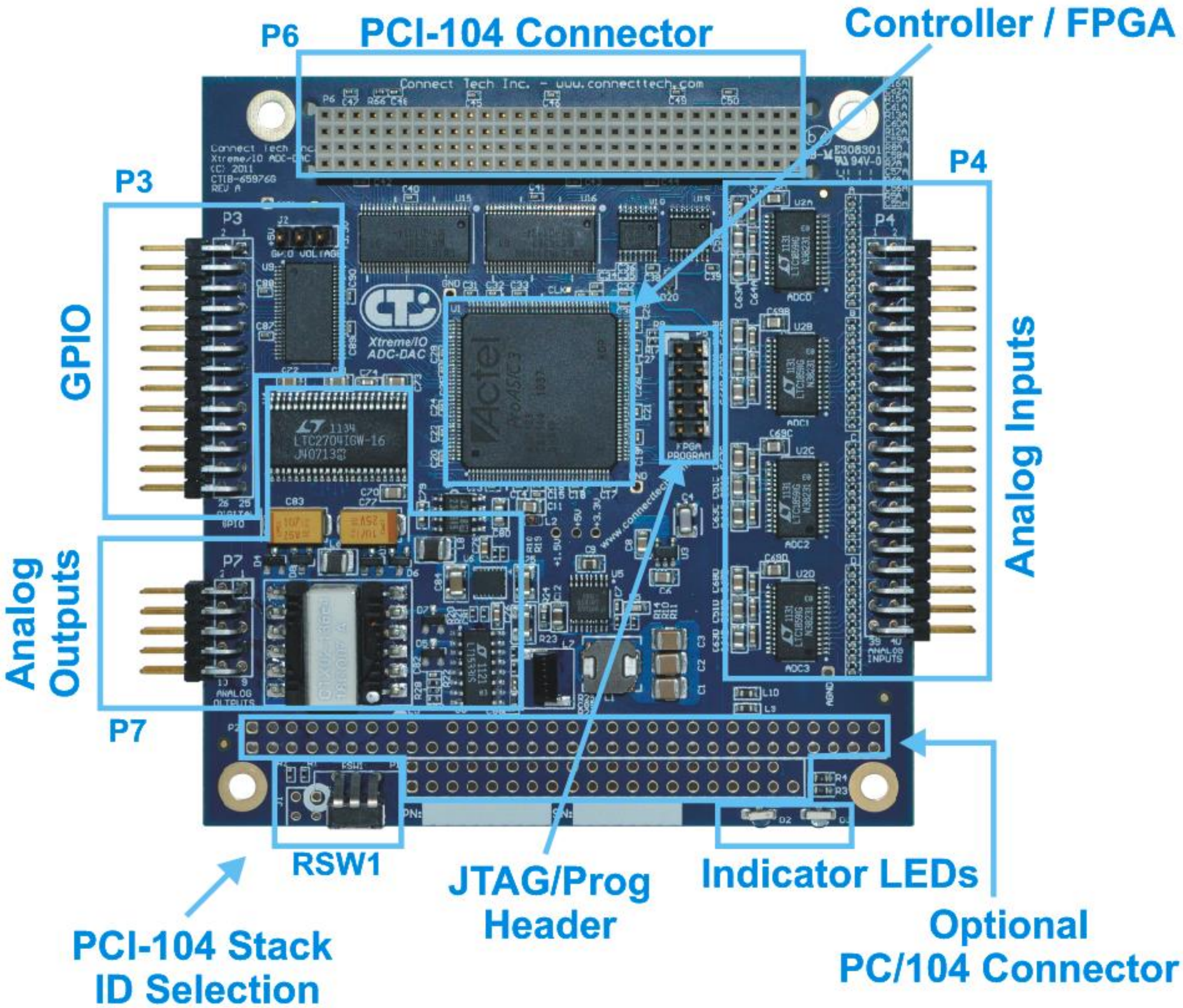
Introduction

Connect Tech's Xtreme I/O ADC-DAC is an analog and digital peripheral board for the PCI-104 small form factor embedded marketplace. This product is ideal for data acquisition, measurement and control applications.

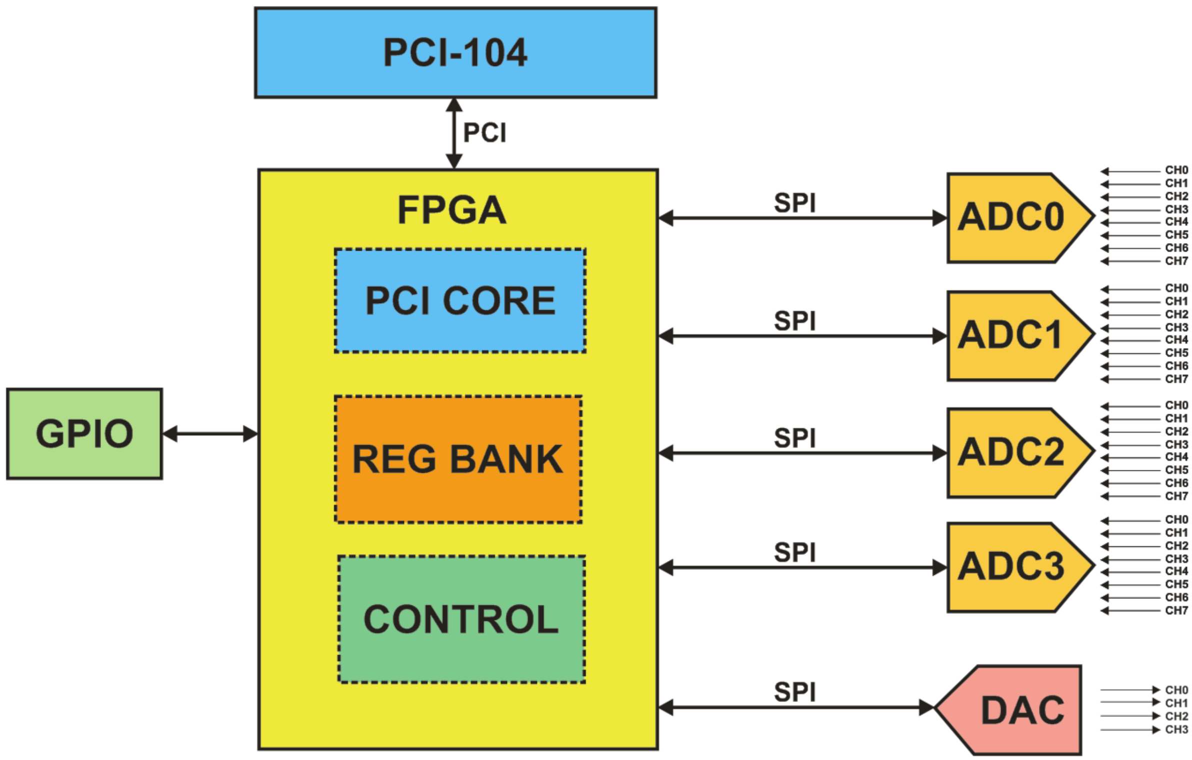
Product Specifcations

Specification	Details
Form Factor	• PCI-104 or PC/104-Plus • Fully PCI 2.0 bus compliant • Jumpers not required for configuration or board detection
Analog Inputs	• **Channels**: 32 Single Ended / 16 Differential • **Resolution**: o DAG003: 16-bit o DAG004: 16-bit o DAG005: 12-bit (low cost option) • **Sampling Rate**: 100ksps • **Calibration**: Built in temperature Auto calibration • **Protection**: ±25V • **Input Ranges**: Software-Programmable Input Ranges: o 0-5V, 0-10V, ±5V, ±10V • **Temperature Range**: 1LSB INL and DNL over: o -40ºC to 85ºC (-40ºF to 185ºF) • **Signal-to-Noise Ratio**: 87dB
Analog Outputs	• **Channels**: 4 • **Resolution**: 16-bit • **Output Ranges**: Six Programmable Output Ranges o Unipolar: 0V to 5V, 0V to 10V o Bipolar: ±5V, ±10V, ±2.5V, –2.5V to 7.5V • **Temperature Range**: 1LSB INL and DNL over full -40ºC to 85ºC (-40ºF to 185ºF) • **Outputs Drive**: ±5mA
Digital I/O	• **Channels**: 16-bit bidirectional I/O • **Input/Output Ranges**: Hardware selectable +3.3V or +5V(TTL/CMOS) • **Output Drive**: High Current 24mA
Controller	• FPGA Register Controlled Device (No jumpers needed) • Custom logic available upon request
Operating Temperature	• -40 to +85 Degrees Celsius
Dimensions	• 3.775" x 3.550" (PC/104 Compliant)
Host Interface Bus	• PCI-104 (PC/104-Plus) • ISA (PC/104) connector can be optionally installed as a pass-through connector
Power Details	• +5VDC only operation (all on-board voltages are made from the +5V rail) • **Current Consumption** (800mA peak, 500mA typical)
Software Compatibility	• Custom CTI Device Drivers for QNX, Linux, Windows • Device can also be controlled directly from a memory mapped register set in any operating system
Warranty and Support	• Lifetime Warranty • Free Technical Support

Board Diagram



Block Diagram



Part Number Information

Part Number	Features	Board Image
DAG003	Analog Inputs : 16-bit 32 SE / 16 Diff Analog Outputs : 16-bit 4 Channels GPIO : 16-bits	
DAG004	Analog Inputs : 16-bit 32 SE / 16 Diff Analog Outputs : None GPIO : 16-bits	
DAG005	Analog Inputs : 12-bit 32 SE / 16 Diff Analog Outputs : None GPIO : 16-bits	

Other available ordering options:

- PC/104 pass-through connector installed
- Vertical pin-headers installed
- PCI-104 ID Selection jumpers installed instead of rotary switch
- GPIO removed completely
- ADC inputs scalable from 32 SE / 16 Diff (max) to 8 SE / 4 Diff (min)

To order any of these part numbers or to inquire about the other available ordering options please contact sales@connecttech.com for further information.

Analog Inputs (ADC's)

Overview

The *Xtreme I/O ADC-DAC* use 4 ADC IC's which are interfaced to the on-board FPGA. Each of these ADC IC's have an 8-channel multiplexer that allow for the sampling of 8 single ended channels or 4 differential channels.

ADC IC Features and Specifications

- Part Number: LTC1859 (DAG003, DAG004) LTC1857 (DAG005)
- Resolution: 16-bit (DAG003, DAG004) 12-Bit (DAG005)
- Sample Rate: 100ksps
- 8-Channel Multiplexer with ±25V Protection
- Software-Programmable Input Ranges: 0V to 5V, 0V to 10V, ±5V or ±10V Single Ended or Differential
- ±3LSB INL for the DAG003 & DAG004, ±1LSB INL for the DAG005
- Power Dissipation: 40mW (Typ)
- Signal-to-Noise Ratio: 87dB (Typ) for the LTC1859

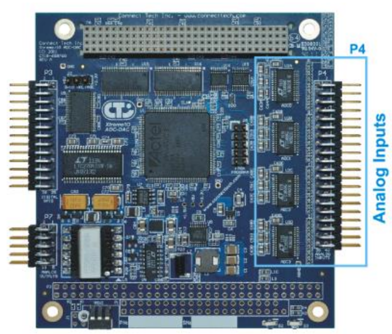
The ADC IC datasheet can be found here: http://cds.linear.com/docs/Datasheet/185789fa.pdf

ADC Connector (P4) Pinout

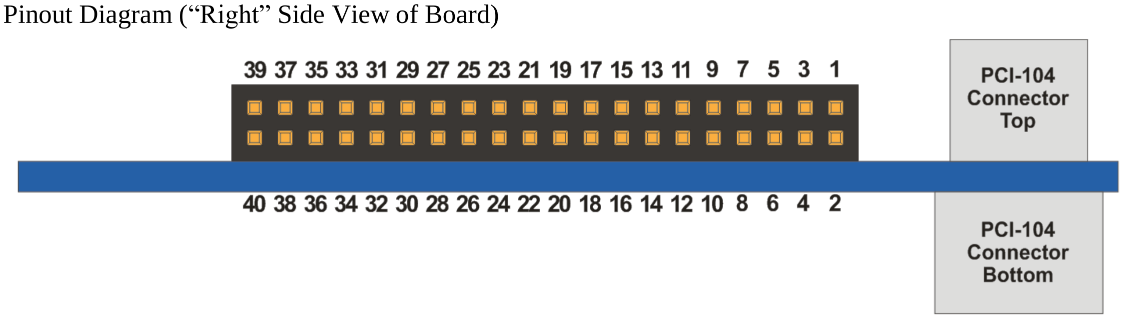
Pinout Table

Signal	HDR Pin	HDR Pin	Signal
ADC0 SE-CH0 / DIFF-CH0+	1	2	ADC0 SE-CH1 / DIFF-CH0-
ADC0 SE-CH2 / DIFF-CH1+	3	4	ADC0 SE-CH3 / DIFF-CH1-
ADC0 SE-CH4 / DIFF-CH2+	5	6	ADC0 SE-CH5 / DIFF-CH2-
ADC0 SE-CH6 / DIFF-CH3+	7	8	ADC0 SE-CH7 / DIFF-CH3-
GND	9	10	*GND*
ADC1 SE-CH0 / DIFF-CH0+	11	12	ADC1 SE-CH1 / DIFF-CH0-
ADC1 SE-CH2 / DIFF-CH1+	13	14	ADC1 SE-CH3 / DIFF-CH1-
ADC1 SE-CH4 / DIFF-CH2+	15	16	ADC1 SE-CH5 / DIFF-CH2-
ADC1 SE-CH6 / DIFF-CH3+	17	18	ADC1 SE-CH7 / DIFF-CH3-
GND	19	20	*GND*
ADC2 SE-CH0 / DIFF-CH0+	21	22	ADC2 SE-CH1 / DIFF-CH0-
ADC2 SE-CH2 / DIFF-CH1+	23	24	ADC2 SE-CH3 / DIFF-CH1-
ADC2 SE-CH4 / DIFF-CH2+	25	26	ADC2 SE-CH5 / DIFF-CH2-
ADC2 SE-CH6 / DIFF-CH3+	27	28	ADC2 SE-CH7 / DIFF-CH3-
GND	29	30	*GND*
ADC3 SE-CH0 / DIFF-CH0+	31	32	ADC3 SE-CH1 / DIFF-CH0-
ADC3 SE-CH2 / DIFF-CH1+	33	34	ADC3 SE-CH3 / DIFF-CH1-
ADC3 SE-CH4 / DIFF-CH2+	35	36	ADC3 SE-CH5 / DIFF-CH2-
ADC3 SE-CH6 / DIFF-CH3+	37	38	ADC3 SE-CH7 / DIFF-CH3-
GND	39	40	*GND*

Connector Location



Pinout Diagram ("Right" Side View of Board)



ADC Operation

For each ADC IC the selection of the channel to be sampled, single vs. different and the input voltage range are all configured through an 8-bit command. Each of these commands is stored in an ADC Command register at byte offsets 0x08 for ADC0, 0x09 for ADC1, 0x0A for ADC2 and 0x0B for ADC3. Once the *Xtreme I/O ADC-DAC* is powered on it continually sends these commands out to the ADC IC's and samples/stores their 16-bit (or 12-bit) codes in 16-bit registers at byte offsets 0x00 for ADC0, 0x02 for ADC1, 0x04 for ADC2 and 0x06 for ADC3. Please refer to the complete memory map table in Section X for more details.

ADC Configuration Commands

Each 8-bit ADC command has the following bit layout:

SGL/DIFF#	ODD SIGN	SELECT		INPUT RANGE		ZEROS	
7	6	5	4	3	2	1	0

The parameters for the ADC commands are described below:

MUX ADDRESS				CHANNEL SELECTION							
SGL/DIFF#	ODD SIGN	SELECT		0	1	2	3	4	5	6	7
0	0	0	0	+	-						
0	0	0	1			+	-				
0	0	1	0					+	-		
0	0	1	1							+	-
0	1	0	0	-	+						
0	1	0	1			-	+				
0	1	1	0					-	+		
0	1	1	1							-	+
1	0	0	0	+							
1	0	0	1			+					
1	0	1	0					+			
1	0	1	1							+	
1	1	0	0		+						
1	1	0	1				+				
1	1	1	0						+		
1	1	1	1								+

Note: Single ended readings are referenced to the GND pins on the P4 connector.

Input Range Details

UNI	GAIN	INPUT RANGE
0	0	-5V to +5V
0	1	-10V to +10V
1	0	0V to +5V
1	1	0V to +10V

ADC Code Conversions

When reading the samples from the ADC's on the *Xtreme I/O ADC-DAC*, they will be 16-bit codes of natural binary format with 1LSB = SCALE/65536.

Code translation examples:

Code = 0000 0000 0000 0000 | Scale = 0 to +5V = 5 | **Therefore sampled Voltage is = 0.0000V**
Code = 1000 0000 0000 0000 | Scale = 0 to +5V = 5 | **Therefore sampled Voltage is = 2.5000V**
Code = 1111 1111 1111 1111 | Scale = 0 to +5V = 5 | **Therefore sampled Voltage is = 4.9999V**
Code = 0000 0000 0000 0000 | Scale = 0 to +10V = 10 | **Therefore sampled Voltage is = 0.0000V**
Code = 1000 0000 0000 0000 | Scale = 0 to +10V = 10 | **Therefore sampled Voltage is = 5.0000V**
Code = 1111 1111 1111 1111 | Scale = 0 to +10V = 10 | **Therefore sampled Voltage is = 9.9999V**
Code = 0000 0000 0000 0000 | Scale = -5 to +5V = 10 | **Therefore sampled Voltage is = -4.9999V**
Code = 1000 0000 0000 0000 | Scale = -10 to +10V = 20 | **Therefore sampled Voltage is = 0.0000V**

ADC Operation Pseudo Code Example A
In this example we will set all 4 ADC's to take a single ended readings from SE-CH0 with an input voltage range of 0 to +10V and then we will read back the values

```
//setup command registers
write DWord 0x8C8C8C8C to offset 0x08
//read from ADC0
ADC0code = read Word from offset 0x00
//read from ADC1
ADC1code = read Word from offset 0x02
//read from ADC2
ADC2code = read Word from offset 0x04
//read from ADC3
ADC3code = read Word from offset 0x06
//you can now continually do as many reads as you would like
```

ADC Operation Pseudo Code Example B
In this example we will set:

- ADC0 to take a differential readings from DIFF-CH1 with an input voltage range of -5V to +5V
- ADC1 to take a single ended readings from CH6 with an input voltage range of 0V to +5V
- ADC2 to take a differential readings from DIFF-CH0 with an input voltage range of -10V to +10V
- ADC3 to take a single ended readings from CH2 with an input voltage range of -10V to +10V

Then every 500ms we will store a sample.

```
//setup command registers
write DWord 0x9404B810 to offset 0x08

//start loop
loop
        //read from ADC0
        ADC0code = read Word from offset 0x00
        //read from ADC1
        ADC1code = read Word from offset 0x02
        //read from ADC2
        ADC2code = read Word from offset 0x04
        //read from ADC3
        ADC3code = read Word from offset 0x06
        wait 500ms
end loop
```

Custom ADC Operation Configuration
As stated the current shipping configuration of the *Xtreme I/O ADC-DAC* is setup for a continuous sampling mode. If your end application requires other functionality such as:

- Onboard Hardware buffering or a particular sample size
- PCI interrupts generated from the board based on a specific sample range or other criteria
- Other functionality not mentioned

Please contact Connect Tech Technical Support (support@connecttech.com) to request a custom configuration and CTI engineering team would be happy to help design a customer configuration for you very quickly.

Analog Outputs (DAC's)

Overview

The *Xtreme I/O ADC-DAC* uses a 16-bit 4-channel DAC IC which is interfaced to the on-board FPGA. Each of the 4 analog output channels from the DAC can be controlled independently from the DAC command register at offset 0x18 (the DAC Command register is 32-bits wide).

DAC IC Features and Specifications

- Part Number: LTC2704 (DAG003)
- Six Programmable Output Ranges:
  - Unipolar: 0V to 5V, 0V to 10V
  - Bipolar: ±5V, ±10V, ±2.5V, –2.5V to 7.5V
- 1LSB INL and DNL Over the Industrial
- Glitch Impulse: < 2nV-sec
- Outputs Drive ±5mA
- Settling Time: 4us min, 10us max (in worst case +/-10V range)
- Power-On and Clear to Zero Volts

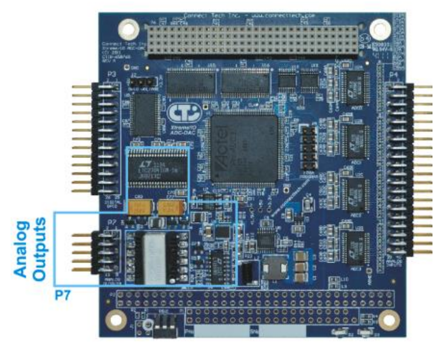
The DAC IC datasheet can be found here: http://cds.linear.com/docs/Datasheet/2704fc.pdf

DAC Connector (P7) Pinout

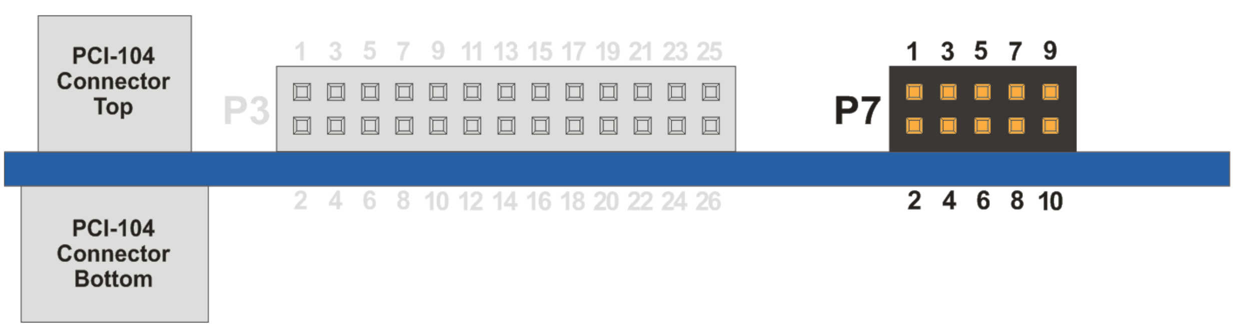
Pinout Table

Signal	HDR Pin	HDR Pin	Signal
DAC_OUTA	1	2	*GND*
DAC_OUTB	3	4	*GND*
DAC_OUTC	5	6	*GND*
DAC_OUTD	7	8	*GND*
GND	9	10	*GND*

Connector Location



Pinout Diagram ("Left" Side View of Board)



DAC Operation

The DAC is controlled directly from a 32-bit DWord DAC command register located at offset 0x18. This command register has two main functions, setting the span value and setting DAC code. Each DAC channel will hold buffer and hold its value until the same DAC is written to again. The command register is described in detail below:

DAC Command Register (offset 0x18)

Zeros								Control				Address				DAC Code or Span															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Control				
0	1	1	0	**Write Span to DAC n**
0	1	1	1	**Write Code to DAC n**
1	0	0	0	**Write Span to all DACs**
1	0	0	1	**Write Code to all DACs**

Address				
0	0	0	0	**DAC A**
0	0	1	0	**DAC B**
0	1	0	0	**DAC C**
0	1	1	0	**DAC D**
1	1	1	1	**All Dacs**

Span																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0V to 5V**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	**0V to 10V**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	**-5V to 5V**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	**-10 to 10V**
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	**-2.5V to 2.5V**
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	**-2.5 to 7.5V**

DAC Code Conversions

When setting the various DAC output voltages for the DAC on the *Xtreme I/O ADC-DAC*, they will be 16-bit codes of natural binary format with 1LSB = SPAN/65536.

Code translation examples:
Code = 0000 0000 0000 0000 | SPAN = 0V to +10V = 10 | **Therefore output voltage will be = 0.0000V**
Code = 1000 0000 0000 0000 | SPAN = 0V to +10V = 10 | **Therefore output voltage will be = 5.0000V**
Code = 1111 1111 1111 1111 | SPAN = 0V to +10V = 10 | **Therefore output voltage will be = 9.9999V**
Code = 0000 0000 0000 0000 | SPAN = -2.5V to +2.5V = 5 | **Therefore output voltage will be = -2.4999V**
Code = 1000 0000 0000 0000 | SPAN = -2.5V to +2.5V = 5 | **Therefore output voltage will be = 0.0000V**
Code = 1111 1111 1111 1111 | SPAN = -2.5V to +2.5V = 5 | **Therefore output voltage will be = 2.4999V**
Code = 0000 0000 0000 0000 | SPAN = 0V to +5V = 5 | **Therefore output voltage will be = 1.2500V**
Code = 0100 0000 0000 0000 | SPAN = 0V to +5V = 5 | **Therefore output voltage will be = 2.5000V**
Code = 1111 1111 1111 1111 | SPAN = 0V to +5V = 5 | **Therefore output voltage will be = 4.9999V**

DAC Operation Pseudo Code Example A

In this example we will set all 4 DAC's to have a span voltage range of 0 to +10V and then set all DAC channel outputs to +10V.

```
//setup span
write DWord 0x008F0001 to offset 0x18
//set output voltages on all DACs
write DWord 0x009FFFFF to offset 0x18
```

DAC Operation Pseudo Code Example B

In this example we will set all 4 DAC's to have a span voltage range of 0 to +10V and then set DAC_OUTA to +0.625V, DAC_OUTB to +1.25V, DAC_OUTC to +2.5V, DAC_OUTD to +5V.

```
//setup span
write DWord 0x008F0001 to offset 0x18
//set DAC_OUTA to +0.625V
write DWord 0x00701000 to offset 0x18
//set DAC_OUTB to +1.25V
write DWord 0x00722000 to offset 0x18
//set DAC_OUTC to +2.5V
write DWord 0x00744000 to offset 0x18
//set DAC_OUTD to +5V
write DWord 0x00768000 to offset 0x18
```

DAC Operation Pseudo Code Example C

In this example we will set DACA span to -5V to +5V, DACB span to 0 to +5V, DACC span to -2.5V to +2.5V and DACD span to -10V to +10V. Then we will set DAC_OUTA to 0V, DAC_OUTB to +3.3V, DAC_OUTC to +2.5V, DAC_OUTD to +5V.

```
//set DACA span to -5V to +5V
write DWord 0x00600002 to offset 0x18
//set DACB span to 0V to +5V
write DWord 0x00620000 to offset 0x18
//set DACC span to -2.5V to +2.5V
write DWord 0x00640004 to offset 0x18
//set DACD span to -10V to +10V
write DWord 0x00660003 to offset 0x18

//set DAC_OUTA to +0V
write DWord 0x00708000 to offset 0x18
//set DAC_OUTB to +3.3V
write DWord 0x0072A900 to offset 0x18
//set DAC_OUTC to +2.5V
write DWord 0x0074FFFF to offset 0x18
//set DAC_OUTD to +5V
write DWord 0x0076C000 to offset 0x18
```

GPIO (Digital I/O)

Overview

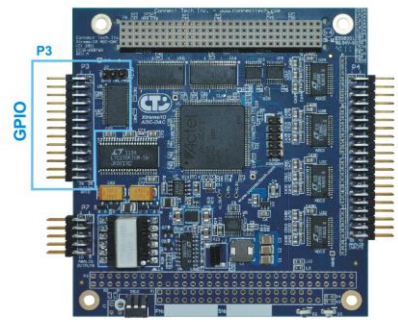
The *Xtreme I/O ADC-DAC* has 16-bits of bi-directional GPIO that can be configured to operate with +3.3V or +5V logic levels. The upper and lower 8 bytes (GPIO0–GPIO7 = lower | GPIO8-GPIO15=upper) can be set to either inputs or outputs independently.

GPIO Connector (P3) Pinout

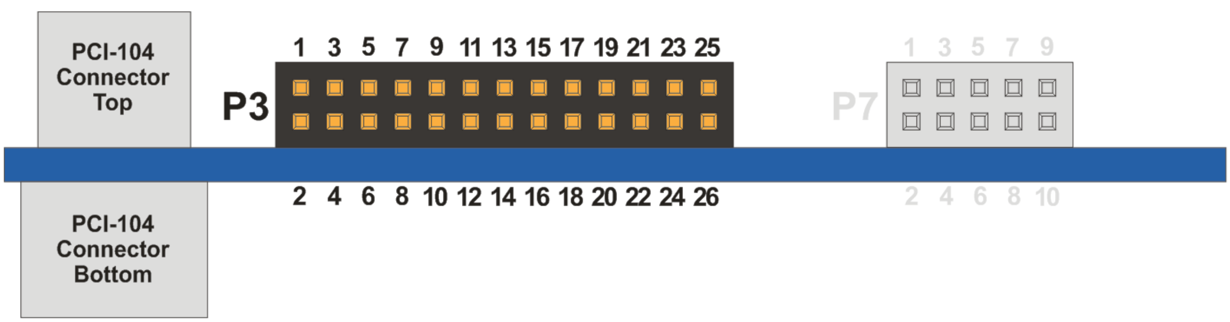
Pinout Table

Signal	HDR Pin	HDR Pin	Signal
GPIO0	1	2	GPIO1
GPIO2	3	4	GPIO3
GPIO4	5	6	GPIO5
GPIO6	7	8	GPIO7
GPIO8	9	10	GPIO9
GPIO10	11	12	GPIO11
GPIO12	13	14	GPIO13
GPIO14	15	16	GPIO15
GND	17	18	*GND*
GND	19	20	*GND*
GND	21	22	*GND*
GND	23	24	*GND*
GND	25	26	*GND*

Connector Location



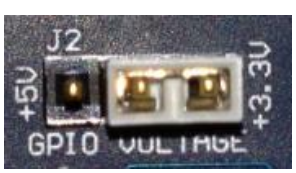
Pinout Diagram ("Left" Side View of Board)



GPIO Voltage Selection Jumper J2



GPIO VOLTAGE = +5V



GPIO VOLTAGE = +3.3V

GPIO Operation

The GPIO operation on the Xtreme I/O ADC-DAC is directly controlled via 3 registers: GPIO_OUT, GPIO_IN and GPIO-MISC_CMD. The register GPIO_OUT at offset 0x0C will set the state of any GPIO pins that are set to outputs. The register GPIO_IN at offset 0x10 will contain the current state of any the GPIO pins that are set to inputs. Any pins that are set to outputs will read a zero value. The input/output directions of the GPIO bits are controlled via the GPIO-MISC_CMD register at offset 0x14.

GPIO OUTPUT Register (offset 0x0C)

Reserved																GPIO OUTPUT															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

GPIO INPUT Register (offset 0x10)

Reserved																GPIO INPUT															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: Each bit corresponds to the GPIO signal on the connector, IE bit-0 = GPIO0 and bit-9 = GPIO9

GPIO-MISC_CMD Register (offset 0x14)

USER LED	Reserved						GPIO8-15 DIR	GPIO0-7 DIR
31	.	.	.	.	3	2	1	0

GPIO0-7 or GPIO8-15 = 0 = **OUTPUTS**
GPIO0-7 or GPIO8-15 = 1 = **INPUTS**

GPIO Operation Pseudo Code Example A

In this example we will set all the GPIO to outputs and the switch all GPIO signals from low to high.

```
//setup GPIO directions
write DWord 0x00000000 to offset 0x14
//set all GPIO signals low
write DWord 0x00000000 to offset 0x0C
//set all GPIO signals high
write DWord 0x0000FFFF to offset 0x0C
```

GPIO Operation Pseudo Code Example B

In this example we will set GPIO0-7 as inputs and GPIO8-15 as outputs, then we will read the GPIO inputs.

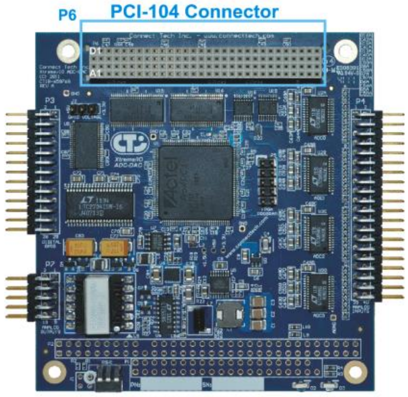
```
//setup GPIO directions
write DWord 0x00000001 to offset 0x14
//read GPIO signals status
GPIO inputs = read Word at offset 0x10
```

PCI-104 Information

PCI-104 Connector Pinout (P6)

Connector P6 is connects to the PCI-104 bus, a full listing of the pinout of the connector is found in the table below.

Connector Location

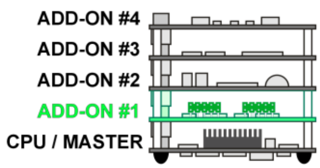
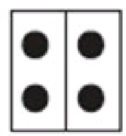
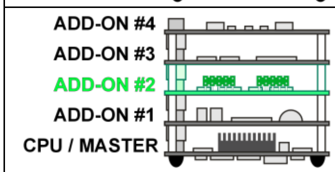
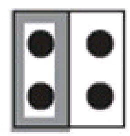
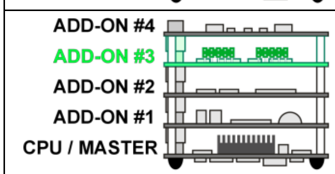
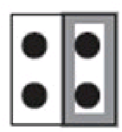
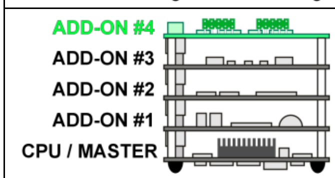
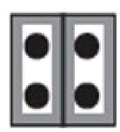


Pinout Table

Pin	A	B	C	D
1	GND	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	Reserved	PAR
10	GND	PERR#	+3.3V	Reserved
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O
24	GND	REQ2#	+5V	GNT0#
25	GNT1#	VI/O	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD#	+5V	RST#
29	+12V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND

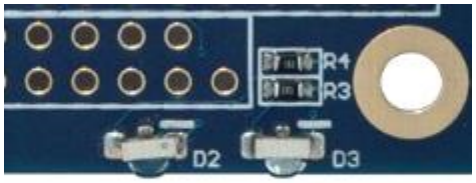
PCI-104 Stack Position Selection

The following PCI signals, (INTA#, INTB# INTC# INTD#), (CLK0, CLK1,CLK2, CLK3), (IDSEL0, IDSEL1, IDSEL2, IDSEL3), are selected by using the jumper block or rotary switch (optionally installed) on the Xtreme I/O ADC-DAC board (J1 / RSW1). Selections need to match the stack location of the Xtreme I/O ADC-DAC in your PCI-104 stack. See the table below for more details.

<table>
<tr><th>Stack Location</th><th>Rotary Switch Setting</th><th>Jumper Block Setting</th><th>PCI INT#</th><th>PCI CLK</th><th>PCI IDSEL</th></tr>
<tr><td>
</td><td>0,4,8,C</td><td></td><td>INTA#</td><td>CLK0</td><td>IDSEL0</td></tr>
<tr><td>
</td><td>1,5,9,D</td><td></td><td>INTB#</td><td>CLK1</td><td>IDSEL1</td></tr>
<tr><td>
</td><td>2,6,A,E</td><td></td><td>INTC#</td><td>CLK2</td><td>IDSEL2</td></tr>
<tr><td>
</td><td>3,7,B,F</td><td></td><td>INTD#</td><td>CLK3</td><td>IDSEL3</td></tr>
</table>

LED Indicators

The *Xtreme I/O ADC-DAC* has 2 indicator LEDs as shown below. LED D2 is the "heartbeat" indicator, the LED should flash on and off continuously to indicate the *Xtreme I/O ADC-DAC* is operating properly. LED3 is intended for user configuration and testing and it is directly mapped to GPIO-MISC_CMD register (offset 0x14) Bit 31.



D2 – Xtreme I/O ADC-DAC "Heartbeat"
D3 – User LED (Mapped to GPIO-MISC_CMD REG Bit 31)

If LED D2 is not flashing at all times when the Xtreme I/O ADC-DAC is powered up please contact Connect Tech Technical Support (support@connecttech.com).

Device Software / Configuration Information

PCI Device Information

The *Xtreme I/O ADC-DAC* product will have the following properties in a PCI system.

PCI Vendor ID: 0x12C4
PCI Device ID: 0x1201
PCI Class Code: 0x0780

The *Xtreme I/O ADC-DAC* has a single register bank which is located in the devices BAR 0 location and is occupies 256 bytes of memory space.

Below is the output from the lspci utility in Linux with a *Xtreme I/O ADC-DAC* installed in the system:

```
00:0d.0 Communication controller [0780]: Connect Tech Inc Device [12c4:1201] (rev 01)
        Control: I/O- Mem+ BusMaster- SpecCycle- MemWINV- VGASnoop- ParErr- Stepping-
SERR- FastB2B- DisINTx-
        Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=slow >TAbort- <TAbort-
<MAbort- >SERR- <PERR- INTx+
        Interrupt: pin A routed to IRQ 18
        Region 0: Memory at db020000 (32-bit, non-prefetchable) [size=256]
```

Device Register Description (Memory Map)

All of the Xtreme I/O ADC-DAC register control set is memory mapped into BAR0 of the PCI device. There are 8 32-bit registers which are used for control and reading of the Xtreme I/O ADC-DAC board. Each of these registered are described in detail in their respective sections throughout this manual, below is a brief overview of all of the registers.

Register Map Overview

REGISTER	READ / WRITE	OFFSET (HEX)	OFFSET (DEC)	REG NUM
ADC01_DATA	R	00	0	0
ADC23_DATA	R	04	4	1
ADC0123_CMD	RW	08	8	2
GPIO_OUT	RW	0C	12	3
GPIO_IN	R	10	16	4
GPIO-MISC_CMD	RW	14	20	5
DAC_CMD	RW	18	24	6
RESERVED	R	1C	28	7

Memory Map Detailed View

<table>
<tr><th>Offset</th><th colspan="32">Register Contents</th></tr>
<tr><td>0x00</td><td colspan="16">ADC1 Code</td><td colspan="16">ADC0 Code</td></tr>
<tr><td>ADC01_DATA</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0x04</td><td colspan="16">ADC3 Code</td><td colspan="16">ADC2 Code</td></tr>
<tr><td>ADC23_DATA</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0x08</td><td colspan="8">ADC3 Command</td><td colspan="8">ADC2 Command</td><td colspan="8">ADC1 Command</td><td colspan="8">ADC0 Command</td></tr>
<tr><td>ADC0123_CMD</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0x0C</td><td colspan="16">Reserved</td><td colspan="16">GPIO OUTPUT</td></tr>
<tr><td>GPIO_OUT</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0x10</td><td colspan="16">Reserved</td><td colspan="16">GPIO INPUT</td></tr>
<tr><td>GPIO_IN</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0x14</td><td>LED</td><td colspan="29">Reserved</td><td>UD</td><td>LD</td></tr>
<tr><td>GPIO-MISC_CMD</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0x18</td><td colspan="8">Zeros</td><td colspan="4">DAC Control</td><td colspan="4">DAC Address</td><td colspan="16">DAC Code or Span</td></tr>
<tr><td>DAC_CMD</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>0x1C</td><td colspan="32">Reserved</td></tr>
<tr><td>RESV</td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
</table>

FPGA Custom Configuration

The Xtreme I/O ADC-DAC product uses the Actel ProASIC3 A3P125 FPGA its main control and configuration unit. Xtreme I/O ADC-DAC ships from Connect Tech with a full featured design pre-loaded into the device. This design allows users to communicate to the control and register portion of the device through the PCI-104 bus. In some situations some customers may find they would like some extra features added into the device that are custom suited for their application. This is where the Xtreme I/O ADC-DAC's FPGA custom configuration can be used.

Connect Tech currently offers two solutions for customers looking to implement a custom FPGA design into the Xtreme I/O ADC-DAC.

Option #1 – Using the Xtreme I/O ADC-DAC Development Kit
Connect Tech offers a full featured development kit that allows experienced FPGA users to design their own HDL to configure the Xtreme I/O ADC-DAC's FPGA.
This development kit includes:
- JTAG Programming Cable
- Full VHDL source code for standard reference design
- Actel Libero IDE Software Suite

Option #2 – Using Connect Tech's Custom Design Services
Connect Tech offers a highly skilled team of engineers with years of experience in custom FPGA designs who can efficiently implement whatever solution you are looking for. To request the teams services please send an email to Connect Tech's sales department (sales@connecttech.com) and they can assist with getting your FPGA project underway.